Fermilab

TM-613
9000.000

CTF BEAM INTERLOCKS

J. C. Gannon

October 9, 1975

Introduction

Attached to this report are several diagrams which show the components of the CTF. Figure 1 is a basic block diagram of the entire CTF system. Figure 2 is a simplified logic diagram of the CTF beam interlocks. Figure 3 is a simplified logic diagram of the low field discriminator. The logic diagram of Figure 4 contains the interface to the Pre-Acc pulse shifter. Figure 5 shows the block diagram of the micro-processor system used in the CTF. Figure 6 is a copy of page 30 on the linac computer which controls and shows the status of the 58^{o} and 32^{o} bending magnet power supplies, sends to and reads from the micro processor the CTF pulsing rate, and displays the status of the CTF Beam Interlocks. Ones, indicate the interlock is made up. A timing diagram showing typical operation of the CTF during HEP operation is included in Figure 7.

The purpose of the CTF beam interlocks are to allow the CTF to run during the time the main ring is not demanding beam. The interlocks also provide a second level of personnel safety in CTF area. The first level is the linac and CTF safety systems.

There are two chassis associated with the CTF beam interlocks. One chassis is located in the Main Control Room at the linac console and the other chassis is located in CTF rack #2 in the linac utility enclosure at area 5. The chassis in the CTF rack contains the 5 volt power supply which supplies the power for both chassis. The status of the system may be monitored at either chassis via LED displays or on page 30 of the linac console. The chassis at the CTF area contains all of the electronics and the MCR chassis is mainly a remote readout and input device. The LED's are organized in groups according to the various levels of interlocks.

Level 1

To receive beam in the CTF, three levels of interlocks must be made up in the CTF beam interlock chassis. Referring to Figure 2, the first level of interlocks enables the 58° bending magnet power supply to ramp. This level of interlocks is controlled by an eight input NAND gate. Presently, only three of these inputs are used and the others are spares. The five spare inputs are connected to a five volt level. The first input to the NAND gate is connected to a RS flip flop. The set input to the flip flop is connected to a channel of a predet in the CTF area which is connected to the experimental clock. When a positive TTL pulse is received at the "T_{ON}" or set input, the output of the flip flop goes high and turns the 58° magnet ramp on, if the other interlocks are made up. This predet is usually set to a time shortly after injection to the main ring. The second input to the RS flip flop is either a "T_{OFF}" timing pulse from the same predet or a TTL level from the pulse shifter interface circuit (Figure 4) which indicates the presence of a HEP beam request. If there is a HEP beam request, which is a high TTL level at the "HEP Beam On" input, the "T_{OFF}" pulse is passed through to the reset input of the flip flop. The output of the flip flop then goes low and turns off the 58° magnet ramp to prepare the linac for injection into the booster. The HEP beam request is determined by a logical combination of all HEP beam switches being on and the linac computer beam enable and either the main ring beam abort being OK OR the 5° bend being in the dump. If there is not a HEP beam request, a TTL low level at the "HEP Beam On" input, the "T_{OFF}" pulse is blocked from reaching the reset input. This action permits the CTF to run constantly when there is no request for HEP beam. If the HEP beam request is turned on after "T_{OFF}" occurs, the circuit waits until the next machine cycle to reset the flip flop and time off the magnet. The output of the flip flop lights a LED in both chassis which are labeled "Timed on." The HEP beam request lights LED's which are labeled "HEP BEAM ON." The other two active inputs to this "LEVEL 1" NAND gates are 24-volt levels which indicate that the linac and CTF enclosures are secured and enabled. These inputs have LED's to indicate their state. They are labeled "LINAC SS" and "Medical SS."

The output of the NAND gate is a low TTL level when all the inputs are a high level. This output is then inverted and sent to the 58° ramp card and into the second level of

beam interlocks. A non-inverted version of this output is sent to the low field discriminator. When all the inputs are present, a HIGH TTL level, a LED is lit in both chassis which are labeled "PS Ramp Enabled."

Level 2

The second level of interlocks consists of another 8 input NAND gate. When all inputs are high, the output goes low and lights LED's in both chassis which are labeled "Beam Ready." This output is then fed to the third level of interlocks.

The first input to the second level is the Q output of a retriggerable one shot with a 100 ms pulse width. The input to the one shot is a 15 Hz strobe pulse from the linac computer. If the strobe pulse disappears for any reason, the one shot times out and the Q output changes from a TTL high to its normal low state and the CTF beam will be inhibited until this strobe pulse returns. The output of the one shot lights LED's in both chassis labeled "Computer Enable" when the strobe pulse is present.

The second input to this level is the output from Level 1 which indicates that the Level 1 interlocks are made up and the power supply ramp is enabled. This input lights a LED in both chassis in the Level 2 area labeled "PS Ramp Enabled."

The pulsing rate of the CTF is determined by the third input. A series of pulses is obtained from the μP during the CTF cycle which sets the number of beam on pulses as well as the number of cycles between the last beam pulse in the train and the first pulse of the next train. These values are set on page 30 of the linac computer. When the μP requests beam, a HIGH TTL level at this input, a LED is lit in both chassis labeled "μP Enable." The μP also looks at the PS ramp enable output and waits ten linac cycles before giving the first "μP Enable" and shuts the enable off as soon as the PS ramp enalbe goes low.

Operator control of the beam may be had at any time by using a beam switch on the MCR chassis. This switch is connected to the fourth input to Level 2. The switch is

labeled "CTF Beam Enable." It lights, when thrown to the on position, a LED next to the switch, and another LED on each of the chassis, in the Level 2 area, labeled "CTF Beam Switch."

Input number five, labeled "Bend Field Nominal" on the LED's, is a level which comes from the μP. The μP looks at the output current of both the 58^{o} and 32^{o} bend power supplies and sends a TTL high level when the currents of both are at their nominal values.

The sixth input is a 24-volt level from the CTF vacuum valve which is downstream of the 58^{o} bend magnet. This level is present when the vacuum valve is open. The LED's associated with this input are labeled "Vacuum Valve."

At present, inputs seven and eight are spares. The LED's associated with them are unlabeled.

Level 3

The Level 2 "Beam Ready" output feeds into Level 3. In Level 3 are two key switches and two output drivers. A key switch is located in each of the chassis. The position of both switches are monitored at each chassis with LED's labeled "CTF Key" and "MCR Key." The LED's light when each key is inserted and turned.

When both keys are turned, the output of Level 2 is passed to the output drivers and if the Level 2 interlocks are made up, a TTL low level at the output of Level 2, a LED on both chassis labeled "CTF Enabled" is lit in the Level 3 area. The Level 2 output is inverted by the Level 3 output drivers and sent to the Pre-Acc pulse shifter and the TANK A pulse shifter. A TTL high at these outputs requests CTF beam from the Pre-Acc and shifts the output RF of Tank 4 out of time with the linac beam. (The energy of Tank 4 beam is not required for the CTF.)

HEP Permit Circuit

The 58^{o} magnet for the CTF is a C magnet located between Tanks 4 and 5 of the linac. When the magnet is at

rest field, the remnant field will steer the linac beam as it passes from Tank 4 to 5. To overcome this problem, a bucking winding was wound along with the normal coils of the magnet. This bucking coil is connected to a power supply which provides current to generate a bucking field to zero the remnant field across the magnet. The magnetic field is monitored by a hall probe which has been placed in the magnets aperature and gaussmeter located in the CTF racks. The computer reads the output of the gaussmeter and by adjusting the bucking coil power supply one may zero the field from the linac control console in the Main Control Room (Page 26).

To prevent accidental steering of the beam if the remnant field is not zeroed and to prevent HEP beam when the CTF 58^{o} magent is ramped on, some additional circuits are used which includes; a Low Field Discriminator circuit and, in the beam interlock chassis, a HEP permit/inhibt alarm circuit.

The Low Field Discriminator, shown in Figures 1 and 3, takes the analog output of the gaussmeter, amplifies it, and compares it with a DC level. If the amplified input is smaller than the DC level, a high TTL level is fed to the output. If the amplified input is larger than the DC level, a low TTL level is seen at the output. There are also timer circuits which will sense a failure in the hall probe or gaussmeter.

The chassis which contains the LFD as well as the gaussmeter and bucking coil supply are located in the CTF racks in the linac lower level. The LFD chassis also has LED's on it which indicates whether the magnet field is too high or the bucking field is too high as well as the output state of the LFD.

The HEP permit output from the LFD is then sent to an alarm circuit in the beam interlock chassis, shown in Figure 2. This signal is passed through and sent to the Pre-Acc pulse shifter interface (Figure 4) where it prevents HEP beam or 15 Hz HEP linac beam if the HEP permit output is a TTL low. This signal does not inhibit CTF beam in any way. Thus, any time the field in the 58^{o} magnet is not zeroed, normal accelerated beam in the linac is inhibited.

As the HEP permit signal passes through the beam interlock chassis, it is sampled by an alarm circuit. This circuit waits approximately one second after CTF T_{OFF}

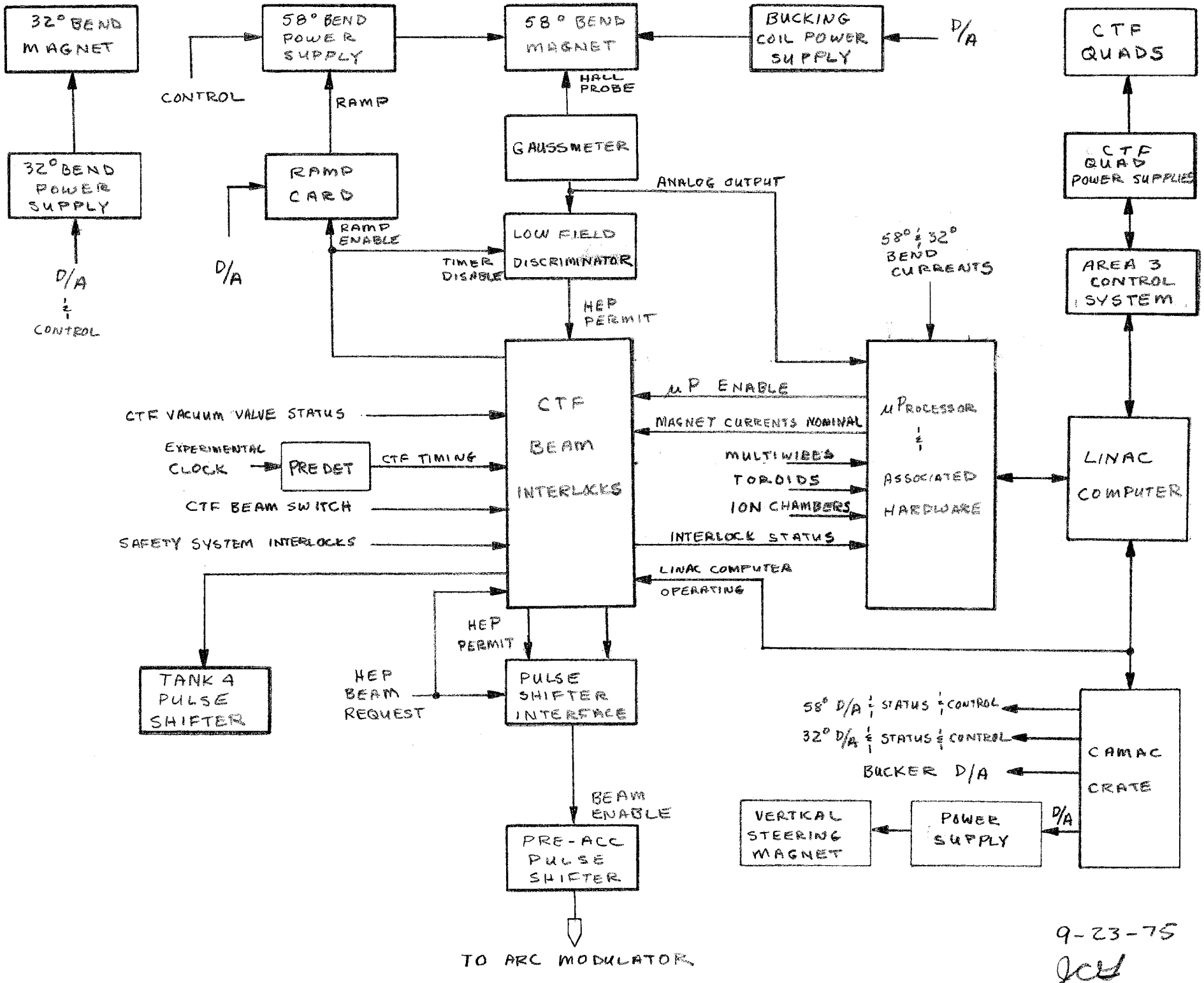
and then looks at the HEP permit signal. If the permit is a TTL low, the alarm circuit sounds a audible alarm in the MCR chassis and flashes a light in both chassis labeled HEP inhibit. The alarm resets automatically when either the HEP permit goes high again or the CTF is timed on.

Summary

For normal operation of the CTF and the HEP program all inputs and outputs to this chassis must be a TTL high level. In the case of the 24-volt inputs, circuitry in the chassis reduces these to TTL high levels. A timing diagram is attached (Figure 7) which shows some of the critical inputs and outputs of the beam interlock chassis.

CTF SYSTEM BLOCK DIAGRAM

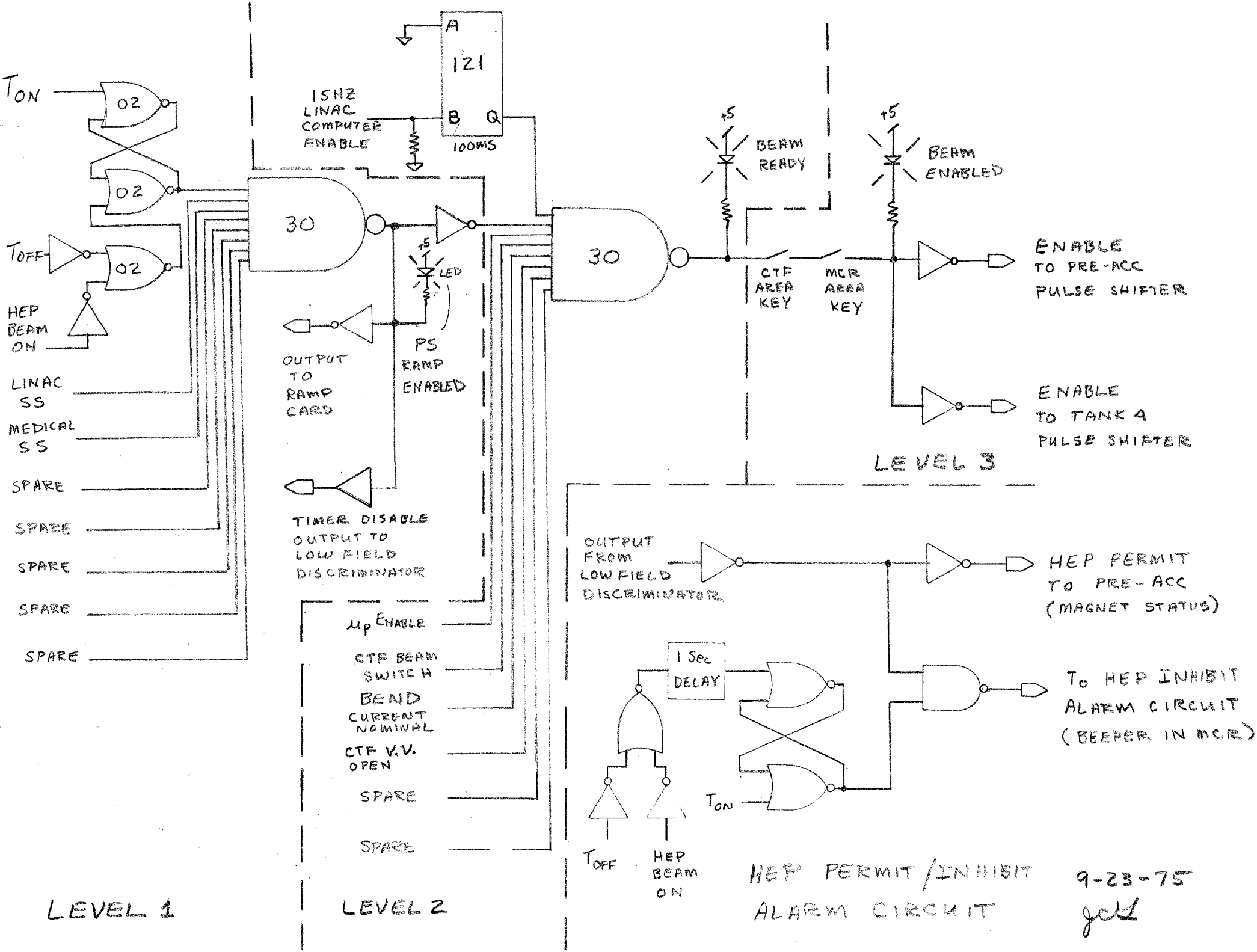
FIGURE 1



9-23-75

JCH

SIMPLIFIED BLOCK DIAGRAM OF CTF BEAM INTERLOCKS FIGURE 2



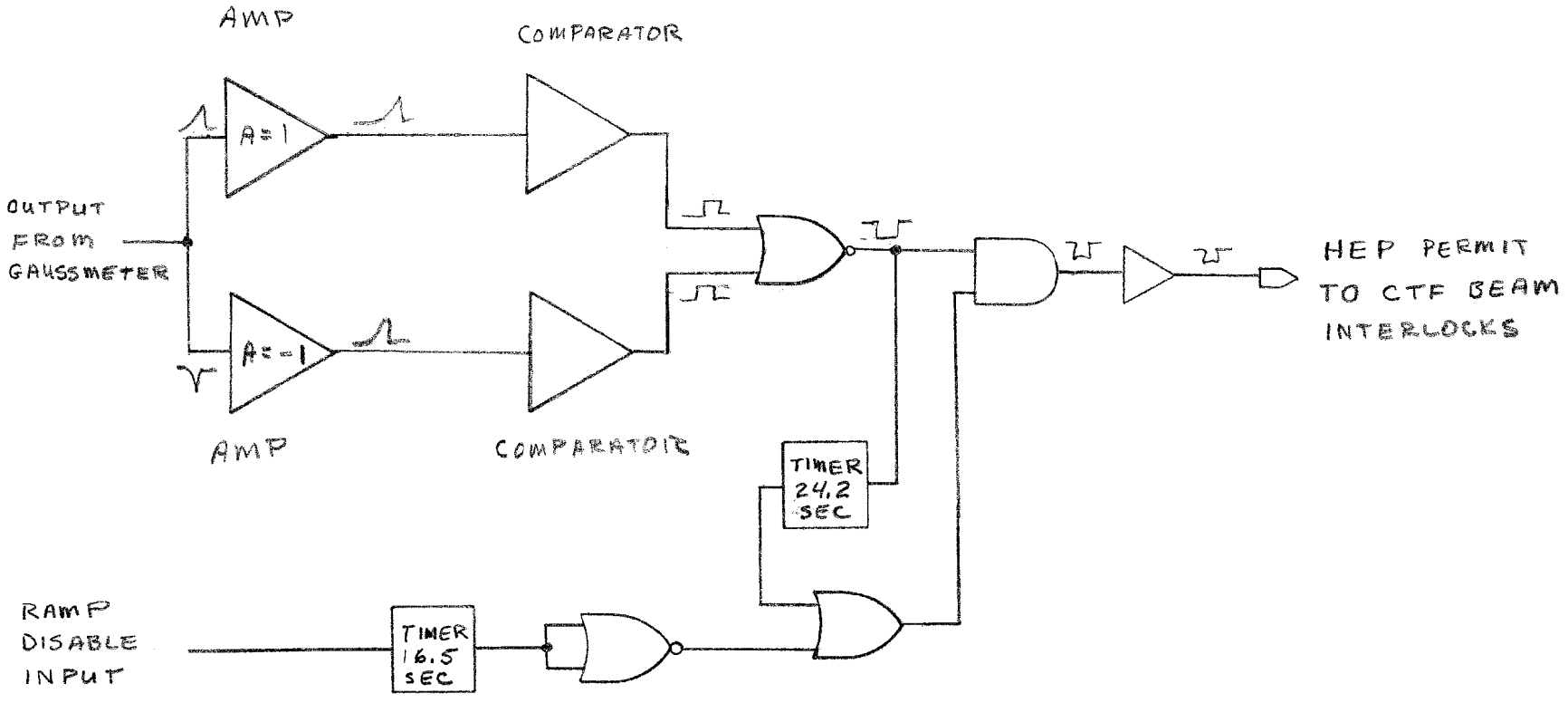
HEP PERMIT/INHIBIT ALARM CIRCUIT

9-23-75

jcl

FIGURE 3

LOGIC BLOCK DIAGRAM OF CTF LOW FIELD DISCRIMINATOR

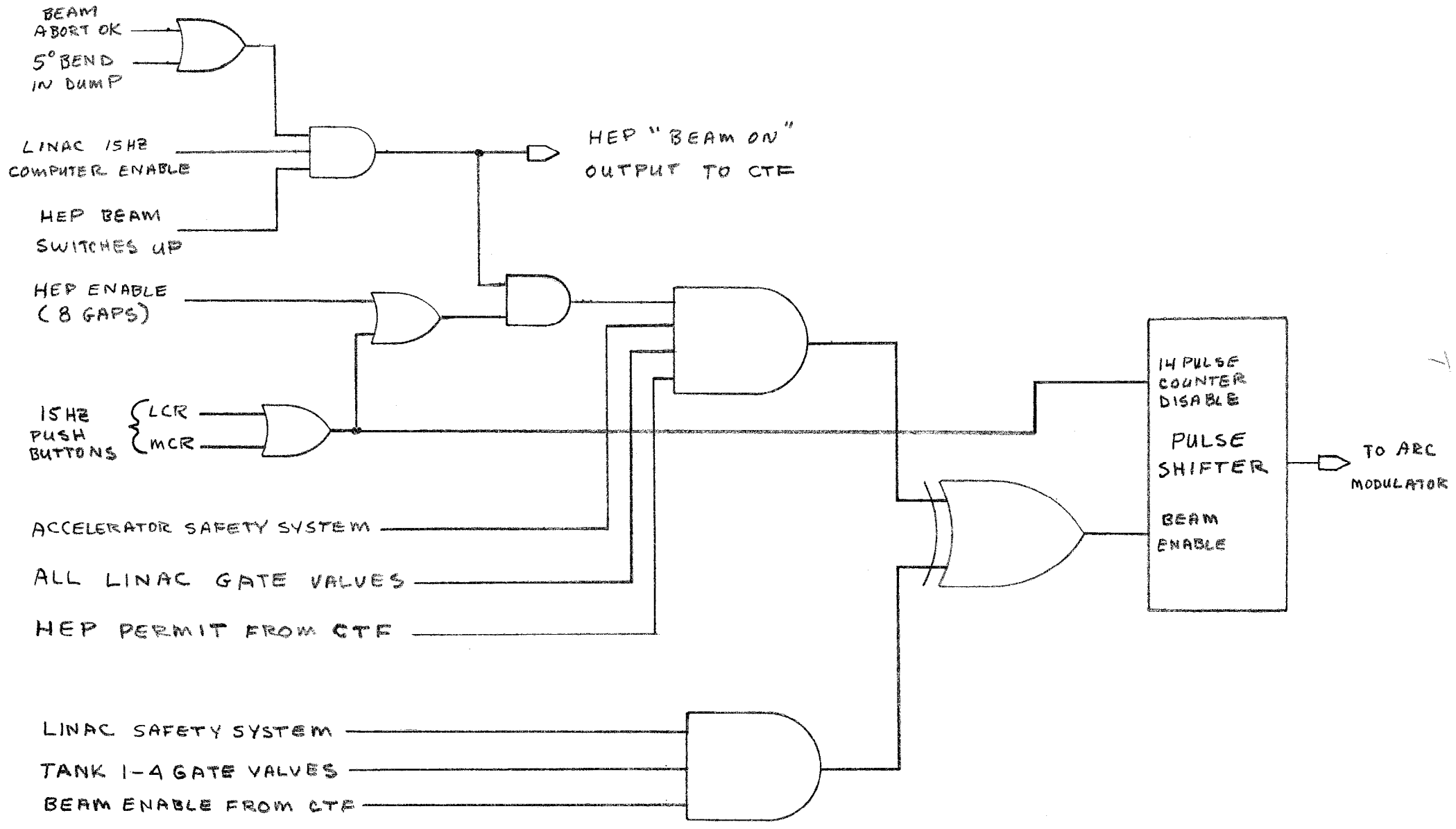


9-23-75

jcb

FIGURE 4

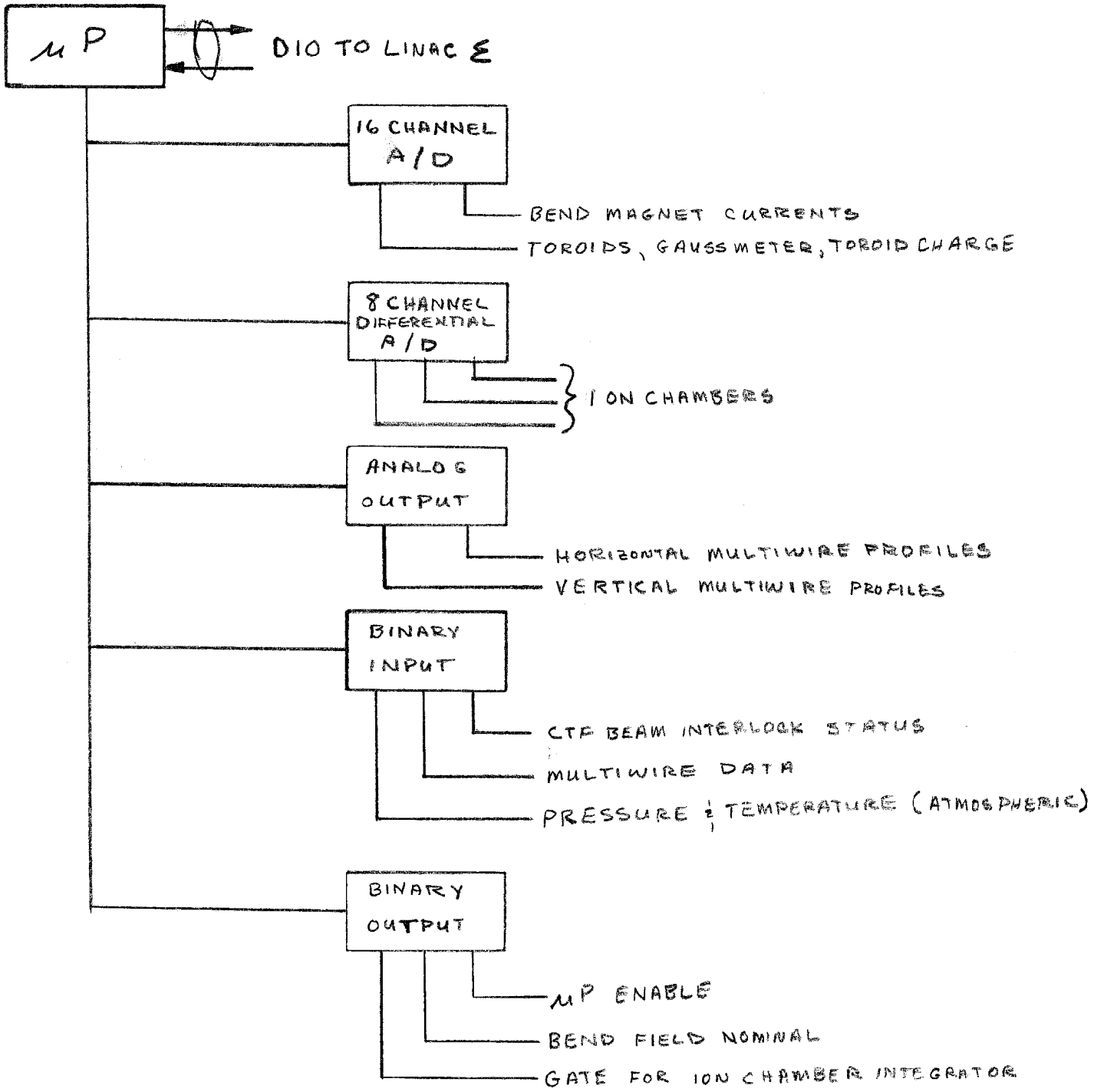
LOGIC BLOCK DIAGRAM OF PRE-ACC PULSE SHIFTER INTERFACE



9-23-75

gcl

CTF μPROCESSOR CONTROL SYSTEM BLOCK DIAGRAM FIGURE 5



9-24-75

FIGURE 6

09/26/75 0928

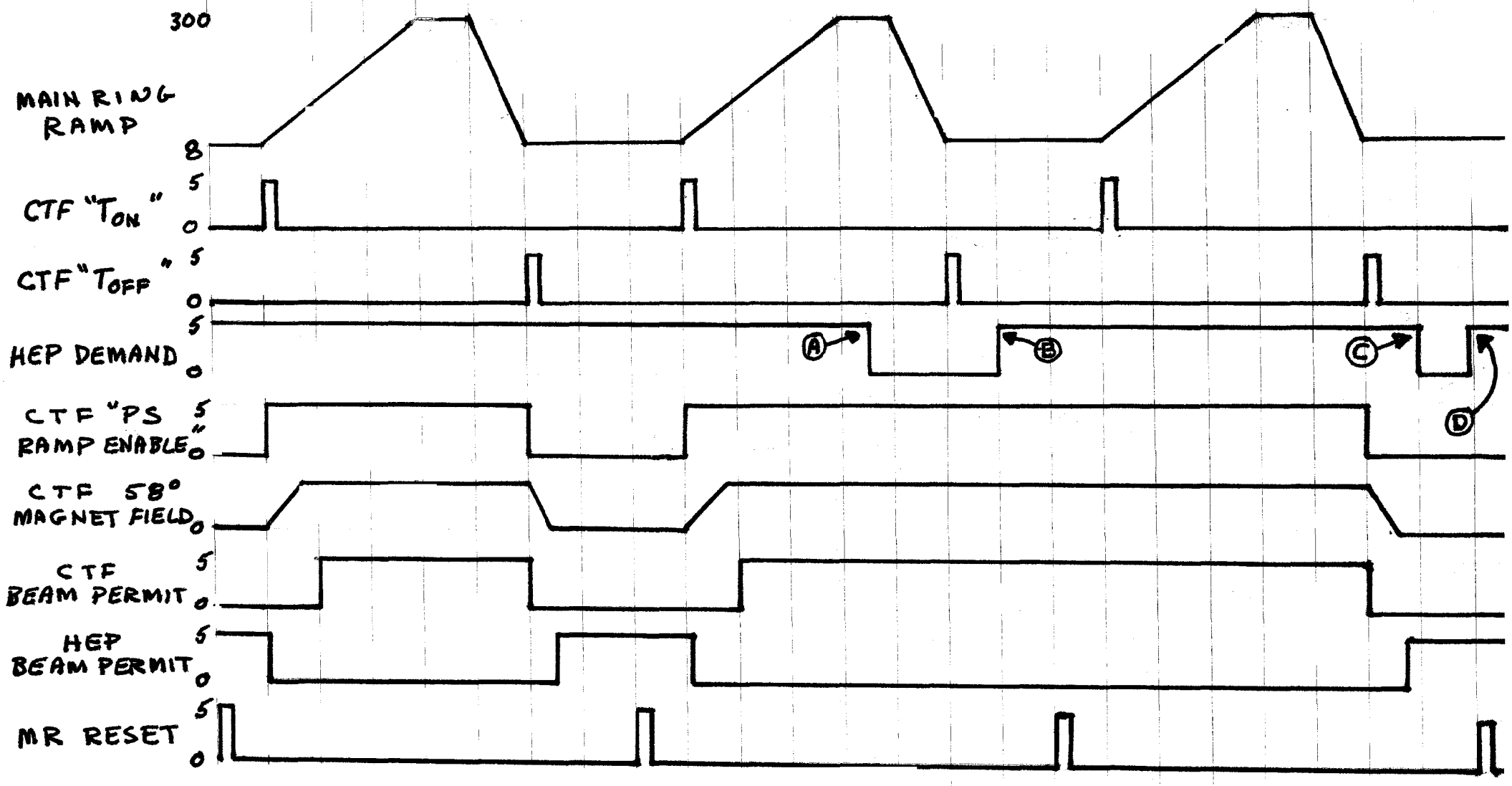
```
30  CTF STATUS
 BEND 58 DEG     .. OFF IL GF DC LF
 BEND 32 DEG     .. OFF IL

*M-P ENABLE: ON=7  OFF=20

BYTE 10=6F                BYTE 11=43
0 CTF PS RAMP ENABL       0 CTF BEAM READY
1 CTF TIMED ON            1 CTF COMP ENABLE
1 LINAC SS                0 CTF M-P ENABLE
0 CTF SS                  0 CTF BEAM SWITCH
1                         0 CTF 58 BEND NOM
1                         0 CTF VAC VALVE
1                         1
1                         1
BYTE 12=00                BYTE 20=81
0 CTF BEAM ENABLED        1
0 CTF MCR KEY             0
0 CTF MEDICAL KEY         0 CTF 58 BEND LOAD
0                         0 CTF 58 BEND OVERC
0                         0 CTF 58 BEND GROUN
0                         0 CTF 58 BEND P.S.
0                         0 CTF 58 BEND INTER
0                         1 CTF 58 BEND REMOT
```

C T F TIMING DIAGRAM

FIGURE 7



NOTES:

(A) BEAM ABORTED OR HEP BEAM SWITCH TURNED OFF.

(B) CONDITION IN NOTE (A) RESET.

(C) HEP BEAM SWITCH TURNED OFF OR LINAC COMPUTER INHIBIT.

(D) CONDITION IN NOTE (C) RESET.